signetics

GN003

Subject: TWIN expansion

The following new products are available for the TWIN:

	12NC	item
1.	9390 281 60000	32K RAM (16K user)
2.	9390 281 70000	48K RAM (32K user)
3.	9390 282 00000	2650A/B Slave
4.	9390 282 10000	2650A/B Twice
5.	9390 282 20000	Real Time Analyser
6.	9390 285 60000	SDOS 4.0 + documentation
7.	9390 285 70000	items 1, 3-6

32K/48K RAM

Purpose

1. To speed up the TWIN memory systeem access time and reduce the number of wait states.
2. To provide error detection.

Features

1. Upto 80K bytes dynamic RAM using Signetics 2690 16K x 1 memory chips.
2. Parity detection.
3. Hidden refresh
4. 256 Byte boot PROM using the Signetics 82S141 512 x 8 PROM.
5. 400ns access time.
6. 900ns cycle time.

2650 A/B SLAVE CARD

Purpose

The purpose of the modified Slave CPU card and TWICE interface module is to allow the emulation of both the 2650A and 2650B series microprocessor on the TWIN Development System. The overall functions of this card are similar to the previous Slave CPU card, except this Slave CPU and the TWICE interface module will function at a clock speed of 2 MHz.

Features

1. Supports 2650A/A-1 2650B/B-1 up to 2 MHz.
2. Force Jump Logic.
3. Priority Interrupt Logic.
4. Memory Protection Logic.

REAL TIME ANALYSER

Purpose

The basic TWIN hardware/software package is capable of supporting the early stages of prototype development in various "Debug" modes. It does not allow the user to monitor the system in real-time, because the slave unit is halted whenever its status is checked or displayed. This product is designed to support a prototype system development effort to the very end, where that system operates in a real-time environment.

Features

1. Real-time Trace of 256 transactions
2. 256 Bytes of Shadow Memory (RAM) for utility programs
3. Memory mapping, 64K in 128 byte blocks.

Real-time Trace

Real-time Trace Logic, when enabled, captures up to 256 bus and user defined transactions of the Slave processor. The content of the Trace memory can be stored and/or displayed on an output device.

Shadow RAM

Shadow RAM is required to hold small programs for the Slave CPU that can not be placed in common memory because they could occupy a space that the user might want to use.

Memory map memory

Memory map memory enables the user to assign any number of 128 byte blocks in the 64K slave memory address space, either to the TWIN common memory or to the user memory.

SDOS 4.0

Purpose

The purpose of a new SDOS release is to fix certain bugs which existed with SDOS 2.0, to support the new hardware products as well as improving the existing commands and functions.

Features

1. Comparing two disk files.
2. Dumping a disk file in hexidecimal format.
3. Moving memory within common or user memory or to/from user prototype memory.
4. Filling user/common Memory with a character or character string.
5. Reading an I/O port or memory location.
6. Writing to an I/O port or memory location.
7. Interfacing with a DATA I-O PROM programmer model 7, 9 or 19.
8. Relocatable Assembler.
9. Macro Pre-processor.
10. Linkage editor.
11. Map memory in common and user segments.
12. Arm real time trace.
13. Dump real time trace.
14. Move debug utilities.