signetics

TWIN
Technical Note
Hardware

Number : HW003A

Subject : Corrections to HW003

Date : 1979-05-16

If the 40 V supply was missing or fuse F1 was blown then the EPROM particularly the 2704/8 types could be damaged.
To overcome this the logic circuit diagram has been altered.
This change does not effect the software in any way.

There were also certain errors and omissions in the appendix of HW003. These have been corrected and updated to include the 40 V check. The old pages should be removed and replaced by the pages attached to this note.

1. Command Decoding

Here the necessary I/O address and operation decoding is made and the appropriate I/O port is selected (for further information see System Reference Manual, chapter 7)

2. I/O Ports

Information is read/written from the I/O ports when the required I/O address is equal to the actual address. (in our case E8 - EF) Written information is first latched into a flip flop before being amplified by the tristate line drivers. Data remains unchanged until either new information overwrites the existing information or a reset is given from the control logic. The output ports 0 to 3 are used as follows:

Port 0	address H'E8'	Control
Port 1	address H'E9'	PROM address lines A0 - A7
Port 2	address H'EA'	PROM address lines A8 - A15 *
Port 3	address H'EB'	PROM data (write)

* only lines A8 - A10 are used for the 2716.

All read ports are non-latched such that the information that is read is only valid at that moment in time.
Only two ports are used:

Port 2	address H'EA'	Status
Port 3	address H'EB'	PROM data (read)

3. Control logic

This logic consists of a sequencer to switch on the power supplies in a particular sequence and to switch off in the reverse sequence. The sequencer can only be switched "on" if the PROM power switch on the front panel is on and a command is given to switch on. The absence of one of these conditions will switch the sequencer off. If the sequencer state change from the "on" to the "off" state then all output port flip flops will be reset with the exception of one signal on the control port, namely RPROM, which will be set. In this way all PROM pins will be at a low level.

The control logic consists further of two re-triggerable monoflops. These monoflops are used to give the basic timing when programming a PROM. This is necessary since the TWIN is interrupt driven and interrupts cannot be inhibited e.g. the operator depresses the **<ESC>** key and the slave is "paused" for an indefinite time.

Any time may be generated, however, by retriggering the monoflop just before the CR time of 0.1 mS has elapsed. A software check on the monoflop state prior to the retrigger pulse is made to check that no interrupt has occurred.

4. Power Supplies

The power supplies are so constructed that they can be switched off. Most have single level outputs and others can be switched between two levels necessary for programming. The following voltages are generated:

VDD	+ 12v	
VCC	+ 5v	
VBB	- 5v	
VPP	+ 5v/+25.2v	
$\overline{PRDG}$	+ 26v	rise and fall time is $\geq$ 0.5uS $\leq$ 2uS
$\overline{CS}$/WE	+ 12v	

Each power supply is basically a 3 pin fixed voltage regulator of the type uA78 or uA79 driven by a series darlington enabling a switch on/off function. A ULN2003 is used to drive the positive power supply darlingtons and provide high voltage isolation. The + 26v supply is additionally switched via a push-pull circuit with a CR delay to meet the rise/fall requirements of the 2704/8. This circuit has a current sink capability which is also required by the 2704/8. The maximum current requirements are given in Fig. 2.
The supply to the power supplies is taken from the stabalized power supplies of TWIN with the exeception of the 40v supply which may either be supplied externally via the aux bus input or derived from the 82S115 PROM card.

	VCC	VBB	VDD	VPP/PROG	$\overline{CS}$/WE
2704/8	10	45	65	20	0.01
2716	100	-	-	30	-

All values in mA

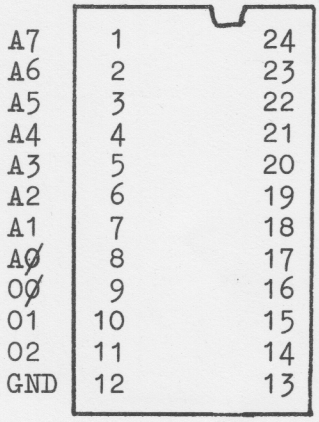
Fig. 2

5. Front Panel

The GP10 board is connected to the front panel PROM R, using the excisting cable which normally connects PROM socket 1 to PR on the 1702A PROM board. Depending on the PROM type to be programmed 2704/8 or 2716 edge connector P4 or P5 should be used respectively.

6. The 2716 EPROM

This PROM is a 16K UV eraseable PROM organized in a 2Kx8 bit matrix operating from a single +5v supply. The pin configuration can be seen in Fig. 3.



AØ-A1Ø	address lines
OØ-07	data lines
PD/PGM	Power down/program
VCC	Power Supply +5v
VPP	Program Voltage

Fig. 3

There are five different modes in which this PROM can operate:

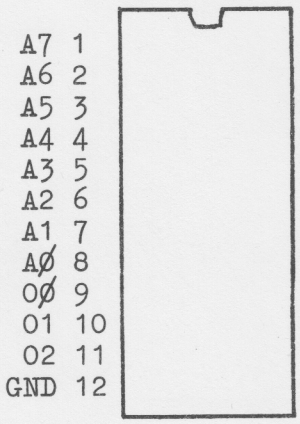
MODE \ PINS	PD/PGM (18)	$\overline{CS}$ (20)	VPP (21)	VCC (24)	OUTPUTS (19-11,13-17)
READ	VIL	VIL	+5	+5	DOUT
DESELECT	DON'T CARE	VIH	+5	+5	HIGH Z
POWER DOWN	VIH	DON'T CARE	+5	+5	HIGH Z
PROGRAM	PULSED VIL TO VIH	VIH	+25	+5	DIN
PROGRAM VERIFY	VIL	VIL	+25	+5	DOUT
PROGRAM INHIBIT	VIL	VIH	+25	+5	HIGH Z

7. Programming

Programming is simple since all signals are TTL compatable. After erasure all bit locations are set to 1's. Programming is accomplished by raising the $\overline{CS}$ input to logic 1 thus selecting the data lines to the input/high impedance-output state. VPP is then raised to 25v ± 1v (in our case 25.2) then the required address together with the required data is supplied. After a minimum of 2 uS setting time a 50 mS programming pulse is applied to the PD/PGM pin. The "next" required address and data is presented and again a pulse is applied. This sequence is then repeated until all locations to be programmed have been selected.
There is no restriction on the address selection sequence nor do all addresses have to be programmed. The only timing requirement with regard to the programming pulse is that the rise and fall times exceed 5nS. This limit will never be reached since this pulse is TTL generated.

8. The 2704/8 EPROM

These EPROMS are both UV eraseable and have a capacity of 4K and 8K organized in a 512x8 and a 1Kx8 matrix. With the exception of capacity both EPROMS are identical and will further be discussed as if one. This EPROM requires 3 power supplies + 5v, + 12v and - 5v. The pinning is shown in Fig. 4.



AØ-A9	Address lines
OØ-07	Data lines
CS/WE	Chip select/write enable
VCC	+5v
VDD	+12v
VBB	-5v
PROGRAM	Program Pulse

✱ connected to GND if 2704

Fig. 4

The three possible operating modes of this EPROM are shown in Fig. 5.

MODE	PIN NUMBER							
	DATA I/O 9-11 13-17	ADDRESS INPUTS 1-8 22,23	VSS 12	PROGRAM 18	VDD 19	$\overline{CS}$/WE 20	VBB 21	VCC 24
READ	DOUT	AIN	GND	GND	+12	VIL	-5	+5
DESELECT	HIGH IMPEDANCE	DON'T CARE	GND	GND	+12	VIH	-5	+5
PROGRAM	DIN	AIN	GND	PULSED 26V	+12	VIHW	-5	+5

Fig. 5

9. Programming the 2704/8

After erasure all bits are in the '1' state. Information is introduced by selectively programming '0's in the required locations.
To program the $\overline{CS}$/WE input is raised to + 12v address 0 is selected and the required information to be programmed is presented to the data pins.
A program pulse is then given. The next sequential address is then selected, the appropriate data is presented to the data pins and again a program pulse is given. This sequence is repeated until all addresses have been programmed.
Depending on the program pulse width the whole sequence must be repeated n times. Since the pulse may be between 0.1 mS and 1 mS and the product of pulse width must be a minimum of 100 mS with a pulse of 1 mS, 100 loops must be made.
Addresses which are not to be programmed should be written with the original information.
The program pulse has a rise/fall time limit of min 0.5 uS and a maximum of 2.0 uS, which means that a CR network has to be used. The pulse may not exceed + 27v and it must have a voltage change of minimum 25v. At its lowest level it must not exceed + 1v while sourceing a maximum of 3 mA.

10. Software

Since a program cannot occupy the same space as ROM information and so as not to limit the maximum capacity of a PROM to be programmed by the slave memory size all ROM information is stored on disk in the form of a binary module. There are three basic functions which are supported:

CP Compare PROM
RP Read PROM
WP Write PROM.

For each function we have two subfunctions:

File handling
PROM read/write routines.

Only the PROM routines vary for different PROMs and functions and the file handling routines vary only for the required function. In this way it is possible to use the same file handling routines together with other PROM routines. This interface will be discussed later. The following routines exist

WP2716	WP2708	WP2704
RP2716	RP2708	RP2704
CP2716	CP2708	CP2704.

Each routine has the following format:

Routine-name Filename A1 A2 A3 C.

For a write command the PROM will be written starting at address A2 and ending at address A3 with the information from the binary file "filename" starting at address A1.
If the complement is required then C must be a 1.
For the read command the PROM will be read from address A2 to A3 and a new file will be created having a load address A1. If the complement information is required then C must be a 1. By loading the file so created and using the dump command a listing of the ROM contents can be obtained.
The following error codes exist:

07	Write error
29	PROM Power not on
34	PROM address range exceeded
52	Incorrect Connector used.

The other errors that may occur are self explanatory.

If another PROM type is to be programmed then a routine having the following interface can be added to the standard routines. The information exchange is via the registers

R0	high order port of the address
R1	low order part of the address
R2	Status
R3	Data.

The status should always be set to a zero unless an error condition occurs. In that case the value filled in by your routine will be displayed on the screen and the program aborted. The routine will be in the form of a subroutine having two or four entry points.

a. Read
b. Read close
c. Write
d. Write end.

For WP all four entry points are required.For CP or RP only the read entry points are needed.
The read end or write end entry point is used to allow your routine to switch off power supplies vect and will always be called in the event of an error.
The entry points addresses are:

Read	H'1000'
Read close	H'1003'
Write	H'1006'
Write end	H'1009'.

A listning of the write routine for the 2716 is given as an example. The source PROM subroutines together with the executable routines and command files is available on a diskette which may be ordered under typenumber 56719, 12NC: 9390.281.10602 costing Hfl. 285.

11. Summary

Although two PROM types have been used here other types may of course be programmed after making the necessary hardware/ software changes.

Appendix to HW003

Remove
B10a and B10b resistor networks

If the power supply is to be mounted on the GP10 board then the connectors A8, A9 and A10 should be removed before any wiring is attempted.
Above the free space so created the seperately constructed power supply can be mounted.

Cut trace non component side (see layout 1)

FROM	TO	REMARKS
A14/7	A14/8	
A13/7	A13/8	
A12/7	A12/8	
D9/15	D10/1	
D11/1	C11/8	
E15/11	E12/15	

Cut trace component side

E7/1	F4/13
A12/16	+ 5v
B8b/4	A10/16

Add a wire non component side

FROM	TO		REMARKS
E12/15	D12/10		
B4/15	D12/10		
E15/11	F4/13		
D11/1	D10/1		RPROM
D10/1	A6/7		RPROM
D12/11	A15/8		
E13/7	A13/10		
A6/1	A12/6		$\overline{\text{PDLOW}}$
A6/2	A12/5		PDHIGH
A6/3	A15/5		SWPON
A6/4	A14/11		RPGM
A6/5	A14/2		SCS
A6/6	A14/10		SPGM
A6/7	A12/3		RPROM
A6/8	A14/3		$\overline{\text{RCS}}$
A9/1	P5-4		CS
A9/6	P5-3		A10
A9/7	P5-6	P4-6	A9
A9/8	P5-7	P4-7	A8

FROM	TO		REMARKS
A7/1	P5-19	P4-19	A7
A7/2	P5-20	P4-20	A6
A7/3	P5-21	P4-21	A5
A7/4	P5-22	P4-22	A4
A7/5	P5-23	P4-23	A3
A7/6	P5-24	P4-24	A2
A7/7	P5-18	P4-18	A1
A7/8	P5-17	P4-17	AØ
A10/1	A10/16		Ø7
A10/2	A10/15		06
A10/3	A10/14		05
A10/4	A10/13		04
A10/5	A10/12		03
A10/6	A10/11		02
A10/7	A10/10		01
A10/8	A10/9		0Ø
A10/1	P5-1	P4-1	07
A10/2	P5-9	P4-9	06
A10/3	P5-10	P4-10	05
A10/4	P5-11	P4-11	04
A10/5	P5-12	P4-12	03
A10/6	P5-13	P4-13	02
A10/7	P5-14	P4-14	01
A10/8	P5-16	P4-16	0Ø
A9/16	A14/4		CSLOW
A9/15	A14/5	P5-2	PD/PGM
A9/13	A15/2		
A9/14	A15/1		
A9/12	A13/15		POWER ON
A14/1	A14/9	A14/8	GND
A14/14	Capacitor		✱
A14/15	Capacitor Resistor Junction		✱
A14/7	Capacitor Resistor Junction		✱
A14/6	Capacitor ✱		
A15/3	A15/4		
A15/6	A13/9		OFF
A13/2	A13/3		+ 3v
A13/3	A9/9		+ 3v
A13/4	A13/14		SWOFFVPP
A13/5	A13/13		SWOFFVCCVDD
A13/6	A13/12		
A13/7	A13/8		GND
A13/11	A15/13		SWONVBB
A15/12	A15/6		OFF
A15/11	A15/10		
A15/9	D2/13		RESET
P5-26	0V		GND
P5-15	0V		GND
P4-25	A4/2		PROM PWR SWCON4
P4-25	A4/4		PROM PWR SWCON5
A4/3	A15/2		
A4/5	A15/1		
A4/1	Collector TR1		

✱ items mounted separately

FROM	TO	REMARKS
P4-15	0V	GND
P4-26	0V	GND
A13/1	A13/2	+ 3v
A12/1	A12/2	SWOFFVCCVDD
A12/1	A13/13	SWOFFVCCVDD
A12/7	A12/4	SWOFF VPP
A13/4	A12/7	SWOFF VPP
A12/13	A12/12	
A12/10	A12/11	

Power Supply Connections

A12/16	Base of Darlington for VDD	
A12/15	Base of Darlington for $\overline{VCC}$	
A12/14	Base of Darlington for $\overline{CS}/WE$	
12/12	Base of Darlington for 26.8v	
A12/10	Base of Darlington for 5v	
A13/11	to PROG control circuit	
VDD	P4-3	
$\overline{VCC}$	P4-8	P5-8
$\overline{CS}/WE$	P4-4	
VBB	P4-5	
PROG	P4-7	
VPP	P5-5	
P1-11/12	+ 12v	input
P1-13/14	- 12v	input
P1-5/6/7/8	+ 40v	input
P1-1/2/3/4	+ 5v	input.

The + 40v supply may either be supplied by an external power supply connected at the rear of the TWIN at the aux bus input and logic ground or a wire has to be connected on the 82S115 PCB from capacitor C27 at E10-11 positive side to P1-5/6/7/8 and fuse F1 changed to a 2A slow blow

Components for GP10

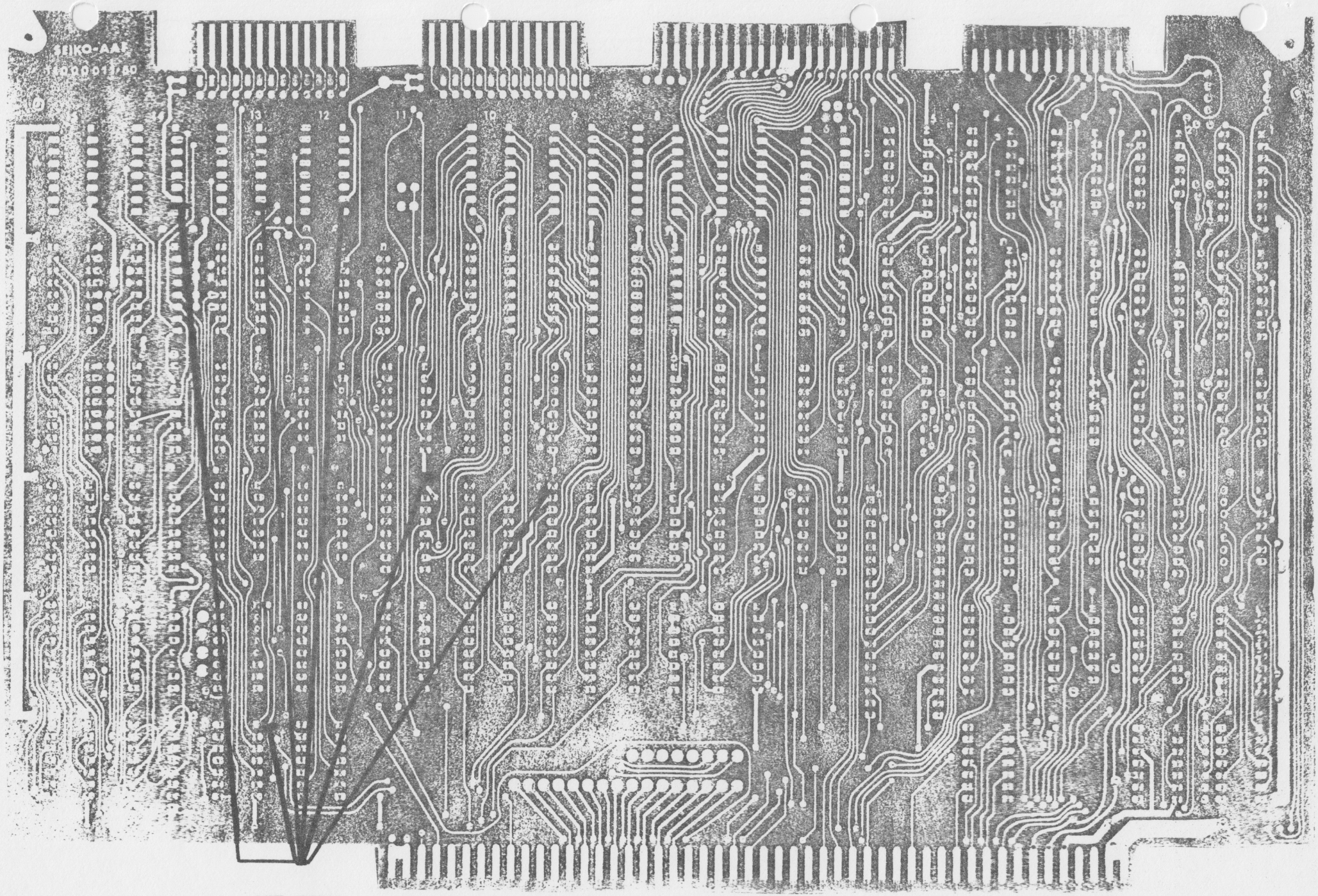
QTY	ITEM	POSITION
1	ULN2003 IC	A 12
1	74195 IC	A 13
1	74123 IC	A 14
1	7400 IC	A 15

QTY	ITEM	DESCRIPTION
1	uA79M05CU	3 pin negative voltage regulator 5 V
2	uA78MHV12CU	3 pin voltage regulator 12 V
1	uA78MHV08CU	3 pin voltage regulator 8 V
1	uA78MHV12CU	3 pin voltage regulator 18 V
2	uA78M05CU	3 pin voltage regulator 5 V
1	7407	I.C.
5	BD331	NPN power darlington
1	BC558	PNP transistor
1	2N2907	PNP transistor
2	2N2222	NPN transistor
12	0.1uF	capacitor 50VWG
1	0.01uF	capacitor 50VWG
5	BYX36	diode
1	BAX13	diode
3	8K2	1/4W resistor
1	3K3	1/8W resistor
2	11K	1/8W resistor
3	10K	1/8W resistor
2	3K	1/8W resistor
1	2K7	1/8W resistor
2	2K2	1/8W resistor
2	39	1/4W resistor
2	5K6	$\frac{1}{4}$W resistor
2	10K pot	variable resistor
2	33000pf	capacitor 6VWG
1	0.68uF	capacitor 10VWG

Adjustments

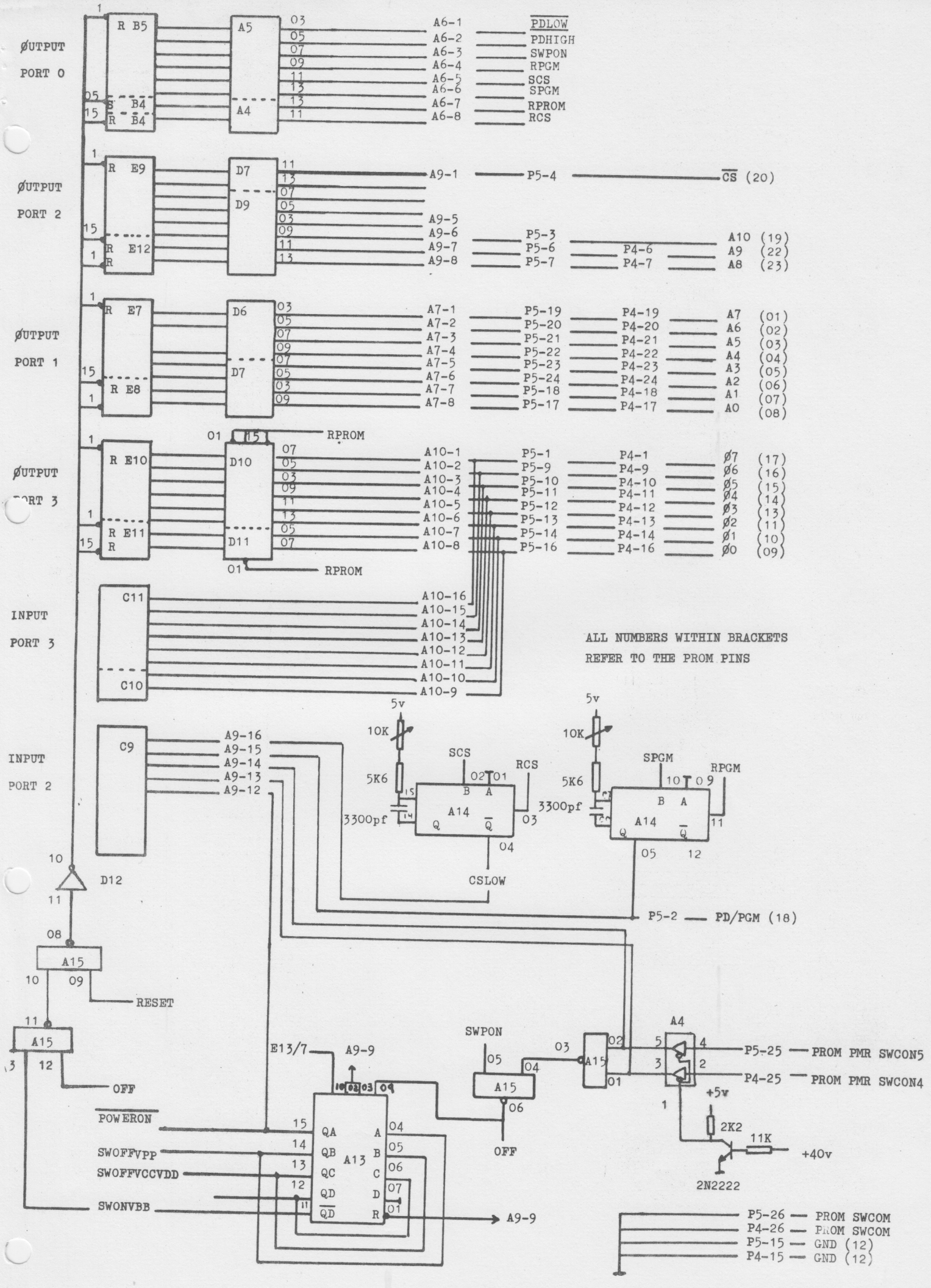
Adjust potmeters to give a pulse of minimum 0.1 mS for PD/PGM and CSLOW.

Note: Although the minimum time constant of 0.1 mS is not critical during normal programming it is, however, important if the program is interrupted. The program pulse length should not then exceed the maximum for the PROM being programmed. This is of course far more critical for the 2704/8 than the 2716 since the maximum program pluse is 1 mS and 55 mS respectively.

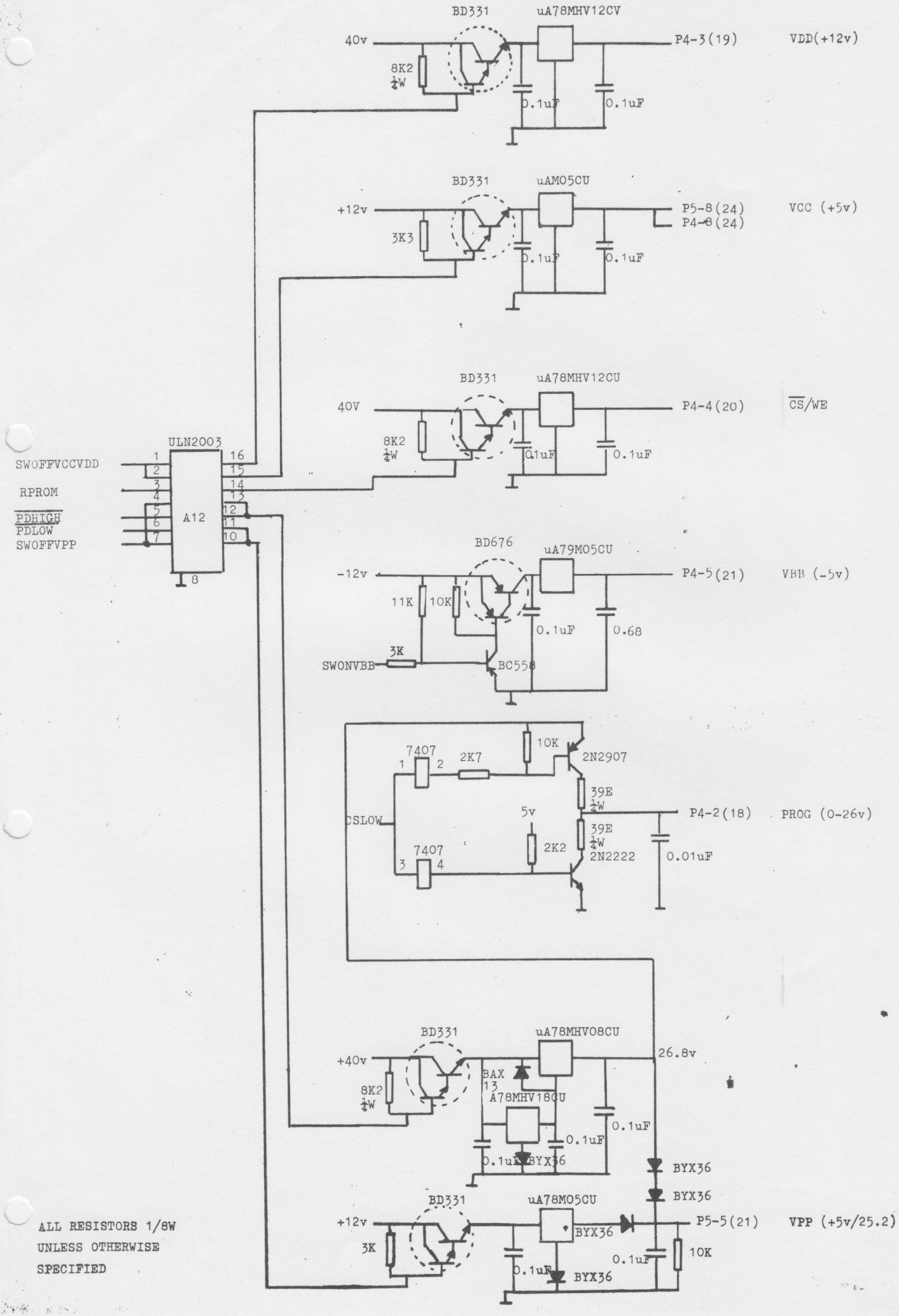


CUT HERE

LAYOUT 1 G.P.I.O. Card

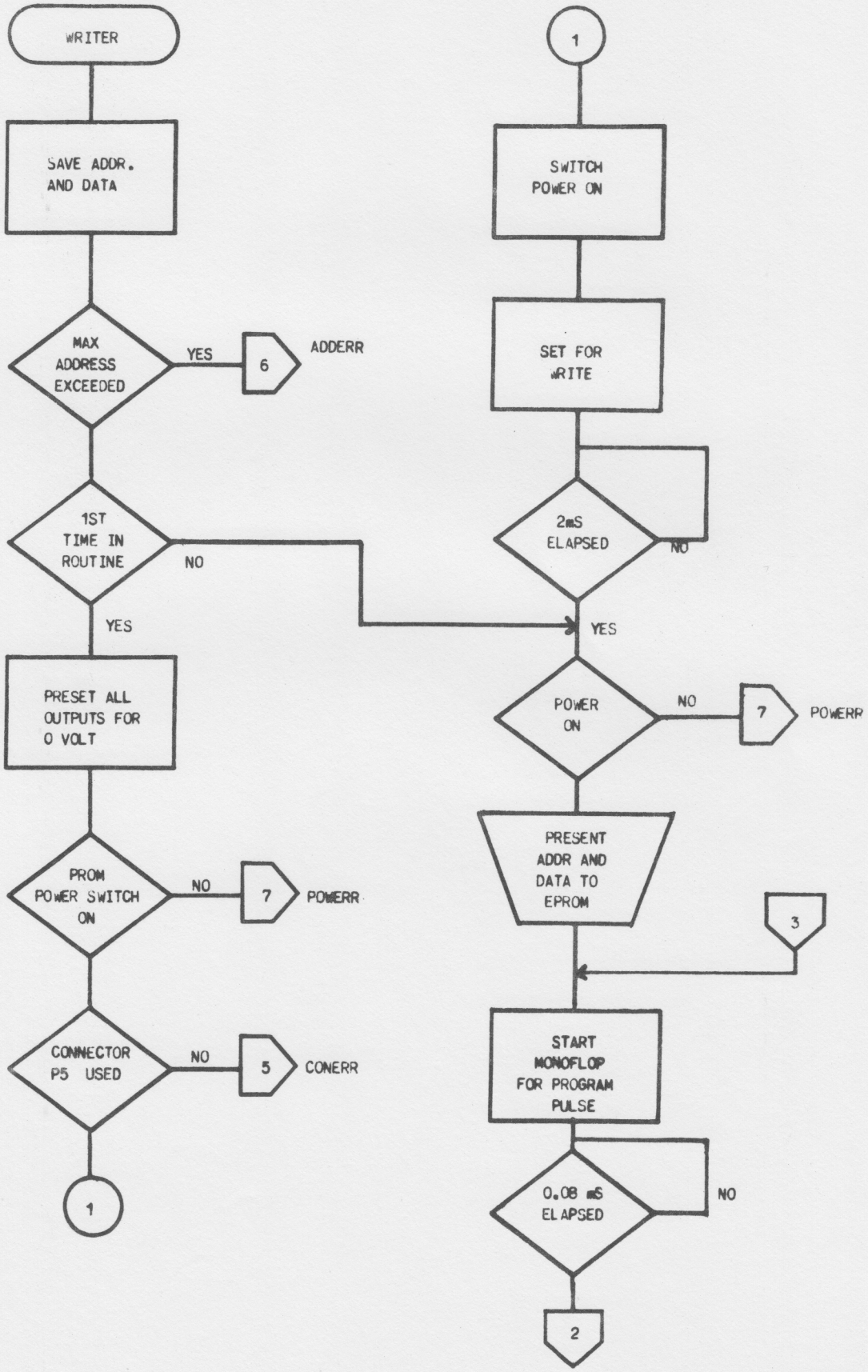

ØUTPUT PORT 0
R B5
A5
A4
S B4
R B4
A6-1 PDLOW
A6-2 PDHIGH
A6-3 SWPON
A6-4 RPGM
A6-5 SCS
A6-6 SPGM
A6-7 RPROM
A6-8 RCS
ØUTPUT PORT 2
R E9
D7
D9
R E12
R
A9-1 P5-4 CS (20)
A9-5
A9-6 P5-3 A10 (19)
A9-7 P5-6 P4-6 A9 (22)
A9-8 P5-7 P4-7 A8 (23)
ØUTPUT PORT 1
R E7
D6
D7
R E8
A7-1 P5-19 P4-19 A7 (01)
A7-2 P5-20 P4-20 A6 (02)
A7-3 P5-21 P4-21 A5 (03)
A7-4 P5-22 P4-22 A4 (04)
A7-5 P5-23 P4-23 A3 (05)
A7-6 P5-24 P4-24 A2 (06)
A7-7 P5-18 P4-18 A1 (07)
A7-8 P5-17 P4-17 A0 (08)
ØUTPUT PORT 3
R E10
D10
R E11
D11
RPROM
A10-1 P5-1 P4-1 Ø7 (17)
A10-2 P5-9 P4-9 Ø6 (16)
A10-3 P5-10 P4-10 Ø5 (15)
A10-4 P5-11 P4-11 Ø4 (14)
A10-5 P5-12 P4-12 Ø3 (13)
A10-6 P5-13 P4-13 Ø2 (11)
A10-7 P5-14 P4-14 Ø1 (10)
A10-8 P5-16 P4-16 Ø0 (09)
INPUT PORT 3
C11
C10
A10-16
A10-15
A10-14
A10-13
A10-12
A10-11
A10-10
A10-9
ALL NUMBERS WITHIN BRACKETS
REFER TO THE PROM PINS
INPUT PORT 2
C9
A9-16
A9-15
A9-14
A9-13
A9-12
5v
10K
5K6
3300pf
SCS
RCS
A14
CSLOW
SPGM
RPGM
P5-2 PD/PGM (18)
D12
A15
RESET
OFF
POWERON
SWOFFVPP
SWOFFVCCVDD
SWONVBB
E13/7
A9-9
A13
SWPON
A4
P5-25 PROM PMR SWCON5
P4-25 PROM PMR SWCON4
+5v
2K2
11K
+40v
2N2222
P5-26 PROM SWCOM
P4-26 PROM SWCOM
P5-15 GND (12)
P4-15 GND (12)

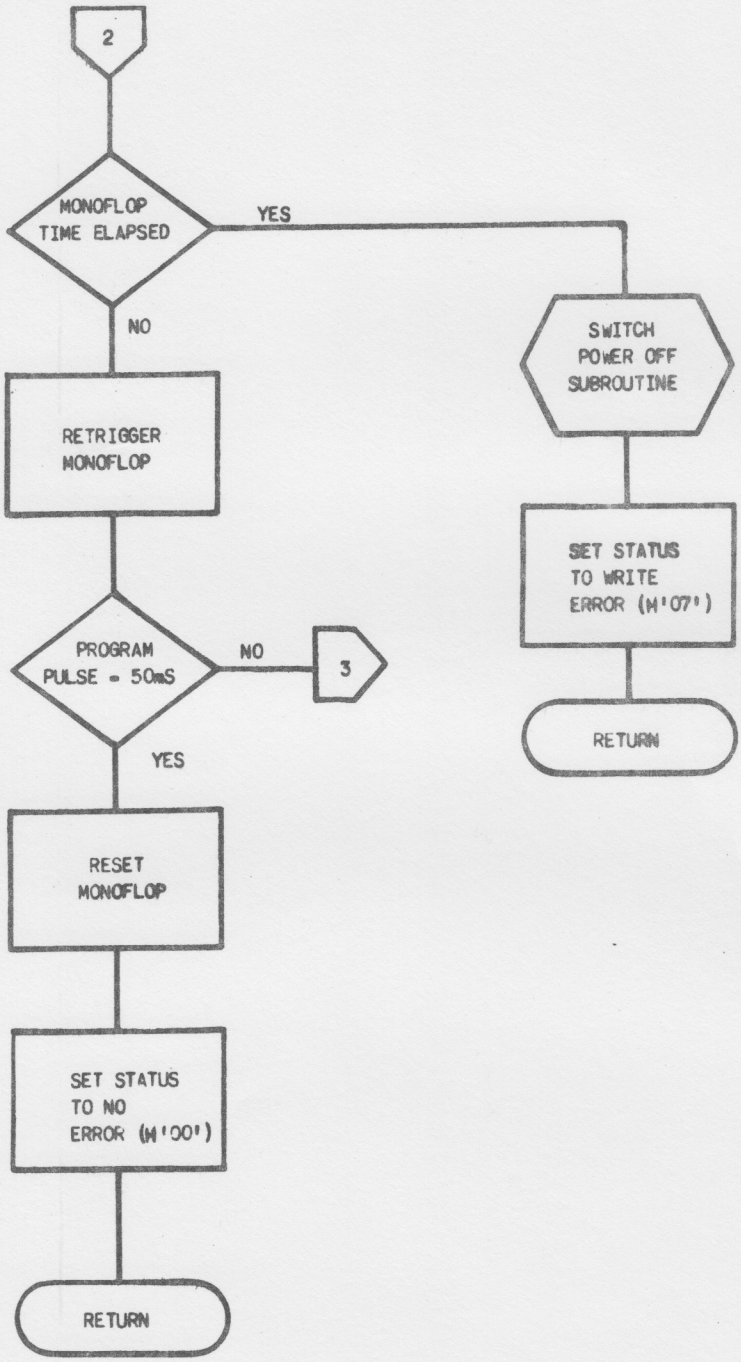
REV A

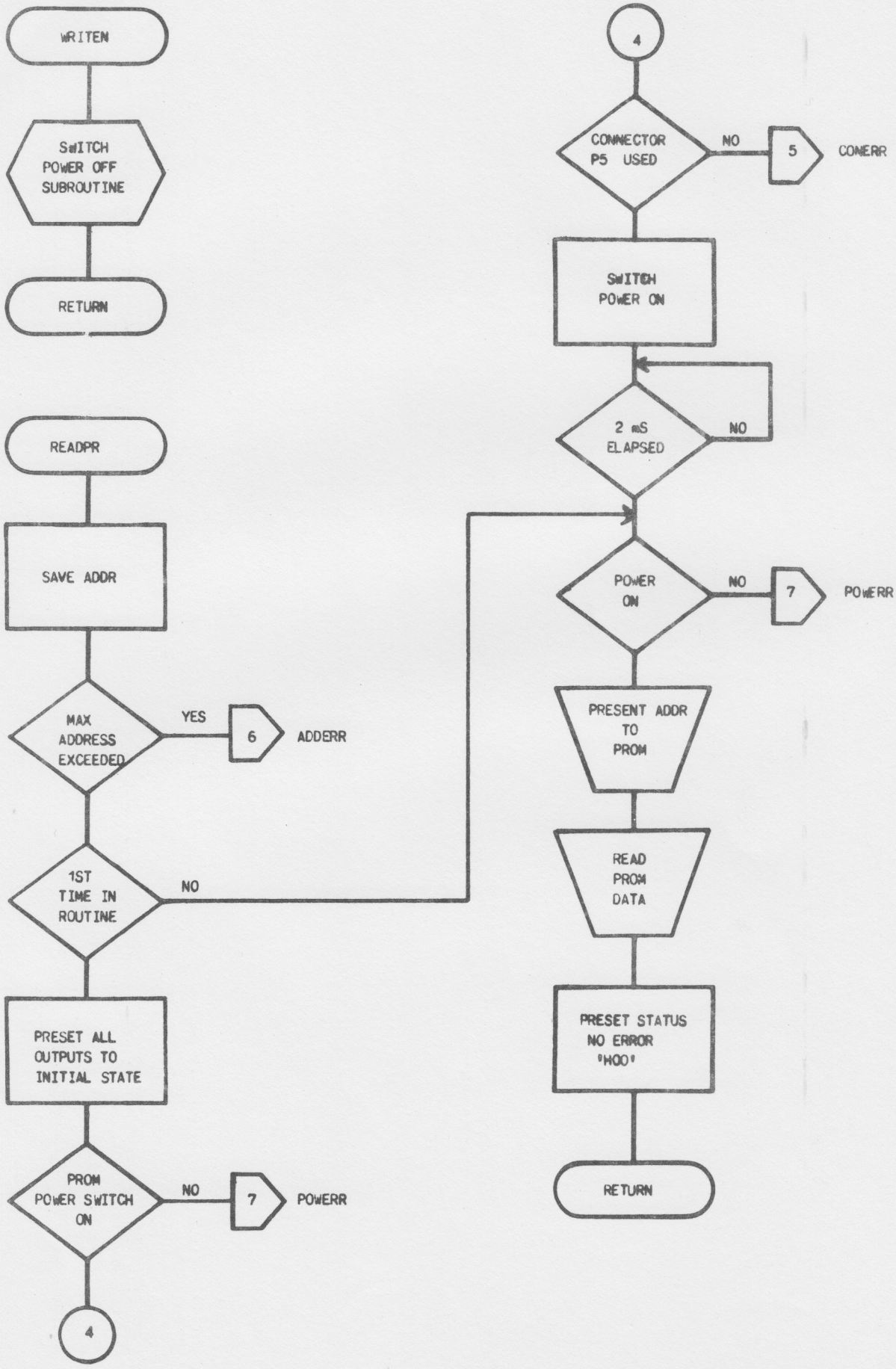


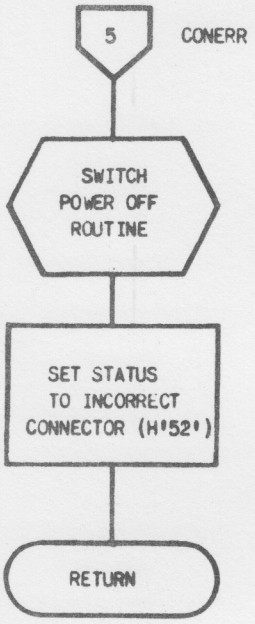
ALL RESISTORS 1/8W
UNLESS OTHERWISE
SPECIFIED

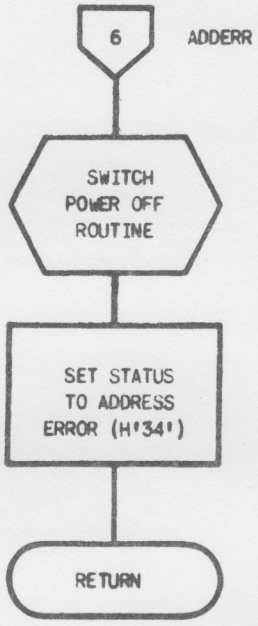
SUBROUTINE WRITE & CHECK A 2716 EPROM

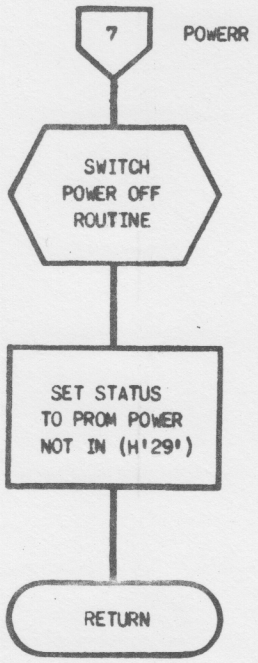


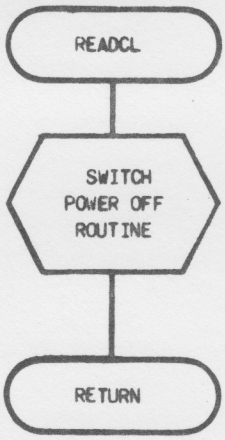

2
MONOFLOP TIME ELAPSED
YES
NO
SWITCH POWER OFF SUBROUTINE
RETRIGGER MONOFLOP
SET STATUS TO WRITE ERROR (H'07')
PROGRAM PULSE = 50mS
NO
3
RETURN
YES
RESET MONOFLOP
SET STATUS TO NO ERROR (H'00')
RETURN


WRITEN
SWITCH POWER OFF SUBROUTINE
RETURN
READPR
SAVE ADDR
MAX ADDRESS EXCEEDED
YES
6
ADDERR
1ST TIME IN ROUTINE
NO
PRESET ALL OUTPUTS TO INITIAL STATE
PROM POWER SWITCH ON
NO
7
POWERR
4
4
CONNECTOR P5 USED
NO
5
CONERR
SWITCH POWER ON
2 mS ELAPSED
NO
POWER ON
NO
7
POWERR
PRESENT ADDR TO PROM
READ PROM DATA
PRESET STATUS NO ERROR 'H00'
RETURN


5
CONERR
SWITCH POWER OFF ROUTINE
SET STATUS TO INCORRECT CONNECTOR (H'52')
RETURN


6
ADDERR
SWITCH POWER OFF ROUTINE
SET STATUS TO ADDRESS ERROR (H'34')
RETURN


7
POWERR
SWITCH POWER OFF ROUTINE
SET STATUS TO PROM POWER NOT IN (H'29')
RETURN


READCL
SWITCH POWER OFF ROUTINE
RETURN

```
LOC OBJECT  ADDR E STMT  SOURCE LINE

                    2  ********************
                    3  * STANDARD SYMBOL DEFINITION - THIS FILE MAY BE APPENDED TO THE
                    4  *                              FRONT OF ANY USER'S SOURCE DECK
                    5  *  REGISTER EQUATES
0000                6  R0      EQU     0       REGISTER 0
0001                7  R1      EQU     1       REGISTER 1
0002                8  R2      EQU     2       REGISTER 2
0003                9  R3      EQU     3       REGISTER 3
                   10  *  CONDITION CODES
0001               11  P       EQU     1       POSITIVE RESULT
0000               12  Z       EQU     0       ZERO RESULT
0002               13  N       EQU     2       NEGATIVE RESULT
0002               14  LT      EQU     2       LESS THAN
0000               15  EQ      EQU     0       EQUAL TO
0001               16  GT      EQU     1       GREATER THAN
0003               17  UN      EQU     3       UNCONDITIONAL
                   18  *  PSW LOWER EQUATES
0000               19  CC      EQU     H'00'   CONDITIONAL CODES
0020               20  IDC     EQU     H'20'   INTERDIGIT CARRY
0010               21  RS      EQU     H'10'   REGISTER BANK
0008               22  WC      EQU     H'08'   1=WITH 0=WITHOUT CARRY
0004               23  OVF     EQU     H'04'   OVERFLOW
0002               24  COM     EQU     H'02'   1=LOGIC 0=ARITHMETIC COMPARE
0001               25  C       EQU     H'01'   CARRY/BORROW
                   26  *  PSW UPPER EQUATES
0080               27  SENS    EQU     H'80'   SENSE BIT
0020               28  II      EQU     H'20'   INTERRUPT INHIBIT
0007               29  SP      EQU     H'07'   STACK POINTER
                   30  * END OF EQUATES
```

TWIN ASSEMBLER VER 2650 WRITE AND CHECK A 2716 PROM

```
LOC OBJECT  ADDR E STMT  SOURCE LINE

                   32  ************************************************************
                   33  *                                                          *
                   34  *                                                          *
                   35  *                WRITE A PROM TYPE 2716                    *
                   36  *                                                          *
                   37  *----------------------------------------------------------*
                   38  *                                                          *
                   39  *       ENTRY POINTS :  WRITPR     WRITE PROM             *
                   40  *                    :  WRITEN     END OF WRITE ROUTINE   *
                   41  *                    :  READPR     READ PROM              *
                   42  *                    :  READCL     END OF READ ROUTINE    *
                   43  *                                                          *
                   44  *       PARAMETERS   :  R0-R1      PROM ADDRESS           *
                   45  *                    :  R2         STATUS RETURN REG      *
                   46  *                    :  R3         BYTE  WRITTEN/READ     *
                   47  *                                                          *
                   48  *----------------------------------------------------------*
                   49  *                                                          *
                   50  *              RETURN STATUS VALUES ARE :                  *
                   51  *                                                          *
                   52  *                00    NO ERROR                            *
                   53  *                07    WRITE ERROR                         *
                   54  *                29    PROM POWER NOT ON                   *
                   55  *                34    PROM ADDRESS RANGE EXCEEDED         *
                   56  *                52    INCORRECT CONNECTOR USED            *
                   57  *                                                          *
                   58  ************************************************************
                   59  *
                   60  *
                   61  *
00E8               62  CONTRO  EQU     H'E8'           CONTROL PORT
                   63  *
0080               64  NPDLOW  EQU     H'80'           PD SET TO 5V NOT
0040               65  NPDHIG  EQU     H'40'           PD SET TO 26V NOT
0020               66  SWPON   EQU     H'20'           SWITCH POWER ON
0010               67  NRPGM   EQU     H'10'           RESET PGM MONO-FLOP NOT
0008               68  NSCS    EQU     H'08'           SET CHIP SELECT MONOFLOP NOT
0004               69  SPGM    EQU     H'04'           SET PROGRAM MODE
0002               70  RPROM   EQU     H'02'           WRITE PROM NOT
0001               71  NRCS    EQU     H'01'           RESET CHIP SELECT MONO-FLOP NOT
                   72  *
                   73  *
00EA               74  STATUS  EQU     H'EA'           STATUS PORT
                   75  *
0080               76  CSLOW   EQU     H'80'           CHIP SELECT LOW (WRITE ENABLED)
0040               77  PGM     EQU     H'40'           PROGRAM MODE PULSE
0020               78  N2716   EQU     H'20'           2716 CONNECTED NOT
0010               79  N2708   EQU     H'10'           2704/8 CONNECTED NOT
0008               80  POWONN  EQU     H'08'           POWER SUPPLIES SWITCHED ON NOT
0007               81  NC      EQU     H'07'           NOT CONNECTED INPUTS
                   82  *
                   83  *
00EA               84  ADDH    EQU     H'EA'           ADRESS HIGH ORDER PORT
                   85  *
0080               86  NCS     EQU     H'80'           CHIP SELECT
```

```
LOC OBJECT   ADDR E STMT  SOURCE LINE

                    87  *
                    88  *
             00E9   89  ADDL    EQU     H'E9'           ADRESS LOW ORDER PORT
                    90  *
                    91  *
                    92  *       ALL OF THE ABOVE SIGNALS WITH THE EXCEPTION OF RPROM
                    93  *        WILL BE RESET TO 0 IF RESET, SWPON, OR PROMPWRN GO TO
                    94  *           ZERO.  RPROM WILL BE SET TO 1
                    95  *
                    96  *
             00EB   97  DATAA   EQU     H'EB'           DATA I-O PORT
                    99  *
                   100  *
1000                101         ORG     H'1000'
             1000   102  READPR  EQU     $
1000 1F10BA  10BA   103         BCTA,UN R2700
             1003   104  READCL  EQU     $
1003 1F10A8  10A8   105         BCTA,UN P2703
             1006   106  WRITPR  EQU     $
1006 1F1012  1012   107         BCTA,UN P2700
             1009   108  WRITEN  EQU     $
1009 1F10A8  10A8   109         BCTA,UN P2703
100C                110  SDATA   RES     1               SAVED DATA BYTE
100D                111  SADD    RES     2               SAVED ADDRESS BYTES
100F                112  STAT    RES     1               STATUS BYTE
1010                113  CON     RES     1               CONTROL INFO BYTE
1011 00             114  FLAG    DATA    0               INITIALIZATION INDICATOR
             0008   115  MAXADD  EQU     <2048           MAXIMUM ALLOWED ADDRESS+1 FOR 2716
```

TWIN ASSEMBLER VER 2650 WRITE AND CHECK A 2716 PROM

```
LOC OBJECT   ADDR E STMT  SOURCE LINE

                   117  *
                   118  *
                   119  *
             1012  120  P2700   EQU     $
1012 CD100E  100E  121         STRA,1  SADD+1
1015 CF100C  100C  122         STRA,3  SDATA
1018 CC100D  100D  123         STRA,0  SADD            SAVE ADDRESS & DATA
101B E408          124         COMI,0  MAXADD          CHECK IF ADDRESS WITHIN LIMITS
101D 9E110E  110E  125         BCFA,LT ADDERR          JIF ERROR
1020 0C1011  1011  126         LODA,0  FLAG            IF INITAILIZED
1023 9C1061  1061  127         BCFA,Z  P2702           JUMP
                   128  *
                   129  *
                   130  *              INITALIZE ROUTINE
                   131  *
                   132  *
1026 04C2          133         LODI,0  NPDLOW+NPDHIG+RPROM
1028 CC1011  1011  134         STRA,0  FLAG            SET INITAILIZED
102B CC1010  1010  135         STRA,0  CON             SAVE INITIAL STATE
102E D4E8          136         WRTE,0  CONTRO          SET INITIAL STATE
1030 54EA          137         REDE,0  STATUS
1032 4470          138         ANDI,0  -1-CSLOW-NC-POWONN REMOVE IRRELEVENT STATUS BITS
1034 E430          139         COMI,0  N2708+N2716     PROM POWER SWITCHED ON
1036 9E111A  111A  140         BCFA,LT POWERR          JIF NOT
1039 E410          141         COMI,0  N2708           INCORRECT CONNECTOR
103B 9C1114  1114  142         BCFA,EQ CONERR          JIF INCORRECT
103E 0C1010  1010  143         LODA,0  CON             GET CONTROL SETTING
1041 6430          144         IORI,0  SWPON+NRPGM     AND
1043 2480          145         EORI,0  NPDLOW
1045 D4E8          146         WRTE,0  CONTRO          SWITCH POWER ON
1047 CC1010  1010  147         STRA,0  CON             SAVE CONTROL SETTING
104A 0403          148         LODI,0  3
104C F87E  104C    149         BDRR,0  $               WAIT 20US
104E 0480          150         LODI,0  NCS             SET FOR WRITE
1050 D4EA          151         WRTE,0  ADDH
1052 0C1010  1010  152         LODA,0  CON             GET CONTROL BYTE
1055 2442          153         EORI,0  RPROM+NPDHIG    & SET FOR WRITE
1057 CC1010  1010  154         STRA,0  CON             SAVE CONTROL BYTE
105A D4E8          155         WRTE,0  CONTRO
105C 07B0          156         LODI,3  176             2MSEC WAIT FOR POWER SUPPLIES TO
105E C0            157  P2701  NOP                       REACH CORRECT LEVEL
105F FB7D  105E    158         BDRR,3  P2701
```

```
LOC OBJECT   ADDR E STMT  SOURCE LINE

                    160  *
                    161  *
                    162  *                WRITE 1 BYTE
                    163  *
                    164  *
             1061   165  P2702   EQU     $
1061 54EA           166          REDE,0   STATUS
1063 24FF           167          EORI,0   H'FF'          INVERT STATUS
1065 F408           168          TMI,0    POWONN         CHECK POWER (STILL) ON
1067 9C111A  111A   169          BCFA,EQ  POWERR         JIF NOT
106A 0C100D  100D   170          LODA,0   SADD          GET HIGH ORDER ADDRESS
106D 6480           171          IORI,0   NCS           KEEP WRITE ON
106F 0D100E  100E   172          LODA,1   SADD+1        GET LOW ORDER ADDRESS
1072 0E100C  100C   173          LODA,2   SDATA         & DATA TO BE WRITTEN
1075 D4EA           174          WRTE,0   ADDH
1077 D5E9           175          WRTE,1   ADDL
1079 D6EB           176          WRTE,2   DATAA          SELECT PROM
107B 0C1010  1010   177          LODA,0   CON           GET CONTROL BYTE
107E 0703           178          LODI,3   3             WAIT 50MS LOOP
1080 066B           179  LOOP3   LODI,2   107
1082 0506           180  LOOP2   LODI,1   6
1084 6404           181          IORI,0   SPGM
1086 D4E8           182          WRTE,0   CONTRO         (RE-)TRIGGER PULSE
1088 2404           183          EORI,0   SPGM
108A D4E8           184          WRTE,0   CONTRO
108C F97E   108C    185  LOOP1   BDRR,1   LOOP1
108E 55EA           186          REDE,1   STATUS
1090 6404           187          IORI,0   SPGM
1092 D4E8           188          WRTE,0   CONTRO         RE-TRIGGER PULSE
1094 2404           189          EORI,0   SPGM
1096 D4E8           190          WRTE,0   CONTRO
1098 F540           191          TMI,1    PGM           CHECK THAT PROGRAM HAS NOT BEEN
109A 9C1120  1120   192          BCFA,EQ  WRIERR         INTERUPTED
109D FA63   1082    193          BDRR,2   LOOP2
109F FB5F   1080    194          BDRR,3   LOOP3
10A1 44EF           195          ANDI,0   -1-NRPGM       RESET MONOFLOP
10A3 D4E8           196          WRTE,0   CONTRO         RESET
10A5 0600           197          LODI,2   0             SET STATUS TO NO ERROR
10A7 17             198          RETC,UN
                    199  *
```

TWIN ASSEMBLER VER 2650 WRITE AND CHECK A 2716 PROM

```
LOC OBJECT   ADDR E STMT  SOURCE LINE

                    201  *
                    202  *
                    203  *                SWITCH OFF ROUTINE
                    204  *
                    205  *
             10A8   206  P2703   EQU     $
10A8 05E0           207          LODI,1   NPDHIG+NPDLOW+SWPON      RESET MONOFLOPS
10AA D5E8           208          WRTE,1   CONTRO
10AC 20             209          EORZ     0                 AND SET FOR READ MODE
10AD C2             210          STRZ     2                 SET STATUS TO NO ERROR
10AE D4E9           211          WRTE,0   ADDL
10B0 D4EA           212          WRTE,0   ADDH
10B2 2520           213          EORI,1   SWPON             SWITCH OFF POWER SUPPLIES
10B4 D5E8           214          WRTE,1   CONTRO
10B6 CC1011  1011   215          STRA,0   FLAG              RESET INITALIZATION FLAG
10B9 17             216          RETC,UN
                    217  *
```

```
LOC OBJECT   ADDR E STMT  SOURCE LINE

             10BA  219  R2700  EQU     $
10BA CD100E  100E  220         STRA,1  SADD+1          SAVE REGISTERS 0 & 1
10BD CC100D  100D  221         STRA,0  SADD
10C0 E408          222         COMI,0  MAXADD          CHECK IF ADDRESS WITHIN LIMITS
10C2 9E110E  110E  223         BCFA,LT ADDERR          JIF ERROR
10C5 0C1011  1011  224         LODA,0  FLAG            IF INITAILIZED
10C8 9C10F6  10F6  225         BCFA,Z  R2702           JUMP
                   226  *
                   227  *              INITALIZE ROUTINE
                   228  *
10CB 0442          229         LODI,0  NPDHIG+RPROM
10CD CC1011  1011  230         STRA,0  FLAG            SET INITAILIZED
10D0 CC1010  1010  231         STRA,0  CON             SAVE INITIAL STATE
10D3 D4E8          232         WRTE,0  CONTRO          SET INITIAL STATE
10D5 54EA          233         REDE,0  STATUS
10D7 4470          234         ANDI,0  -1-CSLOW-NC-POWONN REMOVE IRRELEVENT STATUS BITS
10D9 E430          235         COMI,0  N2708+N2716     PROM POWER SWITCHED ON
10DB 9E111A  111A  236         BCFA,LT POWERR          JIF NOT
10DE E410          237         COMI,0  N2708           INCORRECT CONNECTOR
10E0 9C1114  1114  238         BCFA,EQ CONERR          JIF INCORRECT
10E3 0C1010  1010  239         LODA,0  CON             GET CONTROL SETTING
10E6 6430          240         IORI,0  SWPON+NRPGM     AND
10E8 D4E8          241         WRTE,0  CONTRO          SWITCH POWER ON
10EA CC1010  1010  242         STRA,0  CON             SAVE CONTROL SETTING
10ED 0403          243         LODI,0  3
10EF F87E  10EF    244         BDRR,0  $               WAIT 20US
10F1 07B0          245         LODI,3  176             2MSEC WAIT FOR POWER SUPPLIES TO
                                                          REACH CORRECT LEVEL
10F3 C0            246  R2701  NOP
10F4 FB7D  10F3    247         BDRR,3  R2701
                   248  *
                   249  *
             10F6  250  R2702  EQU     $
10F6 54EA          251         REDE,0  STATUS
10F8 24FF          252         EORI,0  H'FF'           INVERT STATUS
10FA F408          253         TMI,0   POWONN          CHECK POWER (STILL) ON
10FC 9C111A  111A  254         BCFA,EQ POWERR          JIF NOT
10FF 0C100D  100D  255         LODA,0  SADD            GET HIGH ORDER ADDRESS
1102 0D100E  100E  256         LODA,1  SADD+1          GET LOW ORDER ADDRESS
1105 D4EA          257         WRTE,0  ADDH
1107 D5E9          258         WRTE,1  ADDL
1109 57EB          259         REDE,3  DATAA           SELECT PROM
110B 0600          260         LODI,2  0               SET STATUS TO NO ERROR
110D 17            261         RETC,UN
                   262  *
```

TWIN ASSEMBLER VER 2650 WRITE AND CHECK A 2716 PROM

```
LOC OBJECT   ADDR E STMT  SOURCE LINE

             110E  263  ADDERR  EQU     $
110E 3F10A8  10A8  264         BSTA,UN P2703           GO AND SWITCH OFF
1111 0634          265         LODI,2  H'34'           SET INVALID ADDRESS CODE
1113 17            266         RETC,UN
                   267  *
             1114  268  CONERR  EQU     $
1114 3F10A8  10A8  269         BSTA,UN P2703           GO & SWITCH OFF
1117 0652          270         LODI,2  H'52'           SET INVALID DEVICE
1119 17            271         RETC,UN
                   272  *
             111A  273  POWERR  EQU     $
111A 3F10A8  10A8  274         BSTA,UN P2703           GO & SWITCH OFF
111D 0629          275         LODI,2  H'29'           SET INVALID DEVICE
111F 17            276         RETC,UN
                   277  *
             1120  278  WRIERR  EQU     $
1120 3F10A8  10A8  279         BSTA,UN P2703           GO & SWITCH OFF
1123 0607          280         LODI,2  H'07'           SET INVALID DEVICE
1125 17            281         RETC,UN
                   282  *
                   283  *
                   284
                   285         END
                   286  *
                   287  *
                   288  *       TIMING LOOP IS IN CYCLES 12+(X(6.3+Y(42+Z(3.6))))
                   289  *        WHERE X IS R3, Y IS R2 , Z IS R1
                   290  *         Z IS 6 TO GIVE A CONTINUOUS PULSE
                   291  *         SO   12+(X(6.3+Y(42+18))) (0.0024)  MSECS
```

The source PROM subroutine supplied on disc may give a warning if assembled using the relocatable assembler for the source line(s).

```
ANDI,Ø      -1-CSLOW-NC-POWONN
```

The assembler sees this construction as a 2 byte constant having the valve H'FF7Ø'.
The high order byte will be taken giving an incorrect value.

To overcome this problem the source code may be changed so:

```
ANDI,Ø    > -1-CSLOW-NC-POWONN
```

or if prefered:

```
ANDI,Ø    > .NOT.(CSLOW+NC+POWONN)
```