signetics

FUN
Technical Note
Hardware

Number: HW007

Subject: Hang ups when using SDOS 4.0

Date: 1980-11-03

With the introduction of SDOS 4.0 it became possible to map memory, to examine and alter prototype memory etc..
This was possible due to the way in which the ICE mode was used. To obtain data concerning the slave registers and to read prototype memory the debug interface routine is used. This routine resides in the last 256 bytes of slave memory or if the Hardware Analyser Card is present in the ram on that card.
To terminate the interface routine an interrupt is given by using the instruction WRTE,Ø H'FØ.
However, if the ICE mode is set to 1 by the system this instruction will be seen as an instruction for the prototype. Since the I-O address 'FØ' to 'F7' are reserved no action will generally be taken by the prototype. However, OPACK is expected by the system otherwise the system will go into a wait state that cannot be interrupted - if OPACK is tied to 'Ø' volt on the prototype there is no problem. If OPACK is however, generated by the prototype only in the case of valid I-O and memory addresses the system hangs up. To overcome this problem OPACK will automatically be given by the system if an I-O address in the range 'FØ' - 'F7' is given if the following modification to the slave and debug boards are carried out.

On debug PCB

add a wire from P1-79 to P1-91 $\overline{\text{DBGINT}}$
mark modification level to E

On 2650A slave PCB (see Fig. 1)

Cut trace from IC A11 pin 5 to D14 pin 5
Add wire from IC A11 pin 5 to A15 pin 9
Add wire from IC A15 pin 8 to D14 pin 5
Add wire from P1-91 to IC A15 pin 10
Mark modification level to E

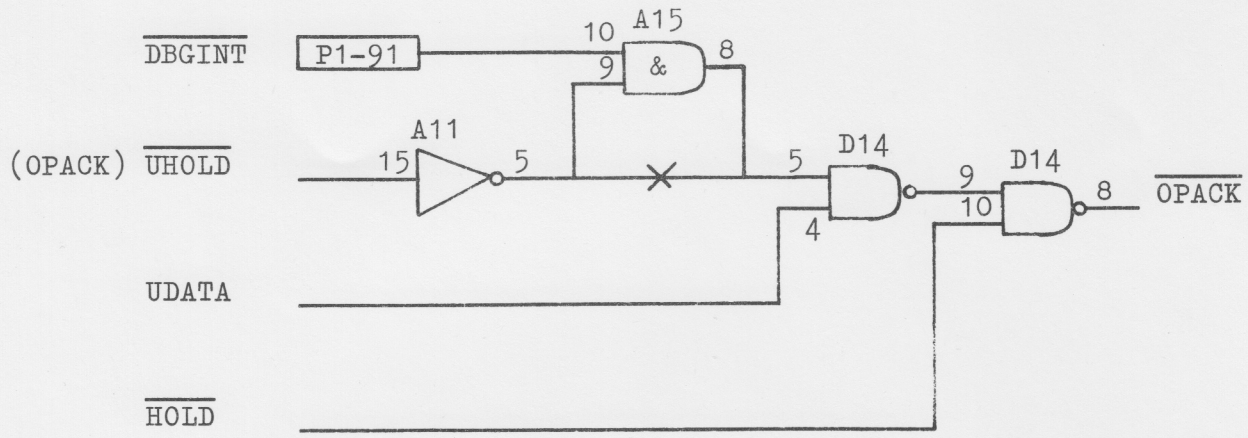


Fig. 1

On 2650 Slave PCB version E to G (see Fig. 2)

Remove IC E-13 (SN7422)

Check that traces to this IC are all cut except VCC and OV

Insert SN7408 in Position E13

Note this is a 14 pin device so a link from either VCC or OV will be necessary.

Cut trace from IC A10 pin 2 to C8 pin 13
Add wire from IC E13 pin 3 to C8 pin 13
Add wire from IC A10 pin 2 to E13 pin 2
Add wire from P1-91 to IC E13 pin 1
Mark modification level to H.

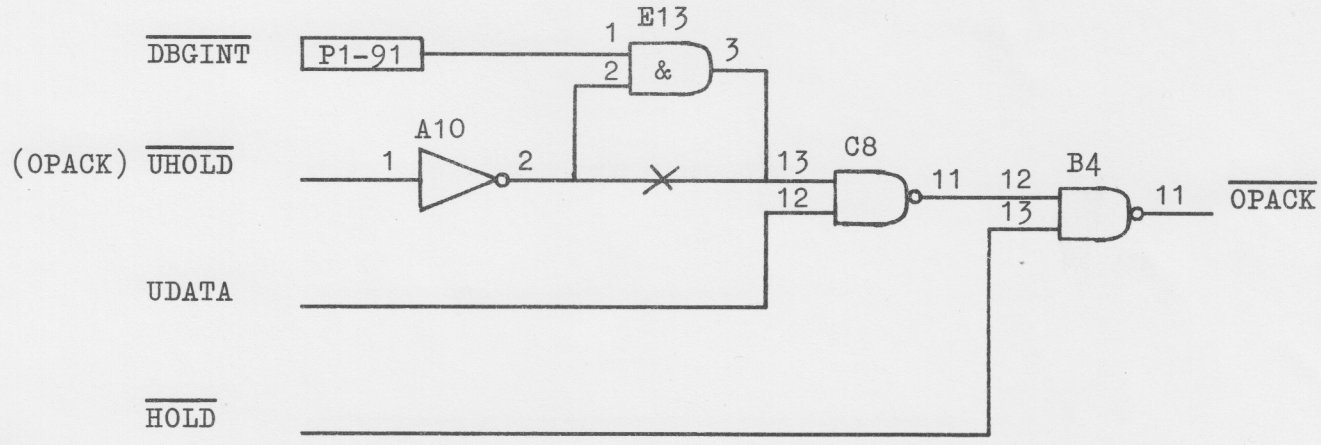


Fig. 2

On 2650 Slave PCB version A (see Fig. 2)

As versions E to G only now E13 is already free.

Mark modification level to B.

NOTE:

During tracing, dumping, etc. the signal OPREQ associated with the instruction WRTE,Ø H'FØ' will still be generated.